# NCP3800V

# SMBus Level 2 Battery Charger

The NCP3800V is a highly integrated Lithium−ion battery charger controller which can be programmed via the SMBus. It can be used to charge smart batteries and includes three loops for output voltage, output current and input current. External switch FETs are driven by internal charge pump drivers.

**Features**

- High Efficiency Current Sense Circuit
- Level 2 SMBus Controlled
- 2/3/4 Cell Li+ Battery
- 25 Volt Maximum Adapter Input Range
- 5.4 V Charge Pump Driving External N−channel FET Switches
- Internal Loop Compensation
- Highly Accurate Regulation
  - ♦ ±0.5% Charge Voltage Accuracy
  - ♦ ±3.5% Charge Current Accuracy
  - ♦ ±3.5% Adaptor Current Accuracy
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**Typical Applications**

- Notebook Computers
- Netbook Computers
- Tablet PCs

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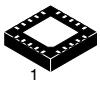


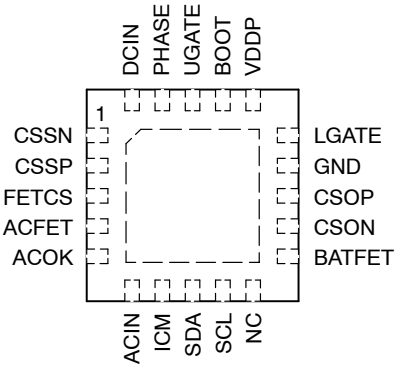

**QFN20**
**MN SUFFIX**
**CASE 485CP**

**MARKING DIAGRAM**


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**PIN CONFIGURATION**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP3800VMNTXG | QFN20 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

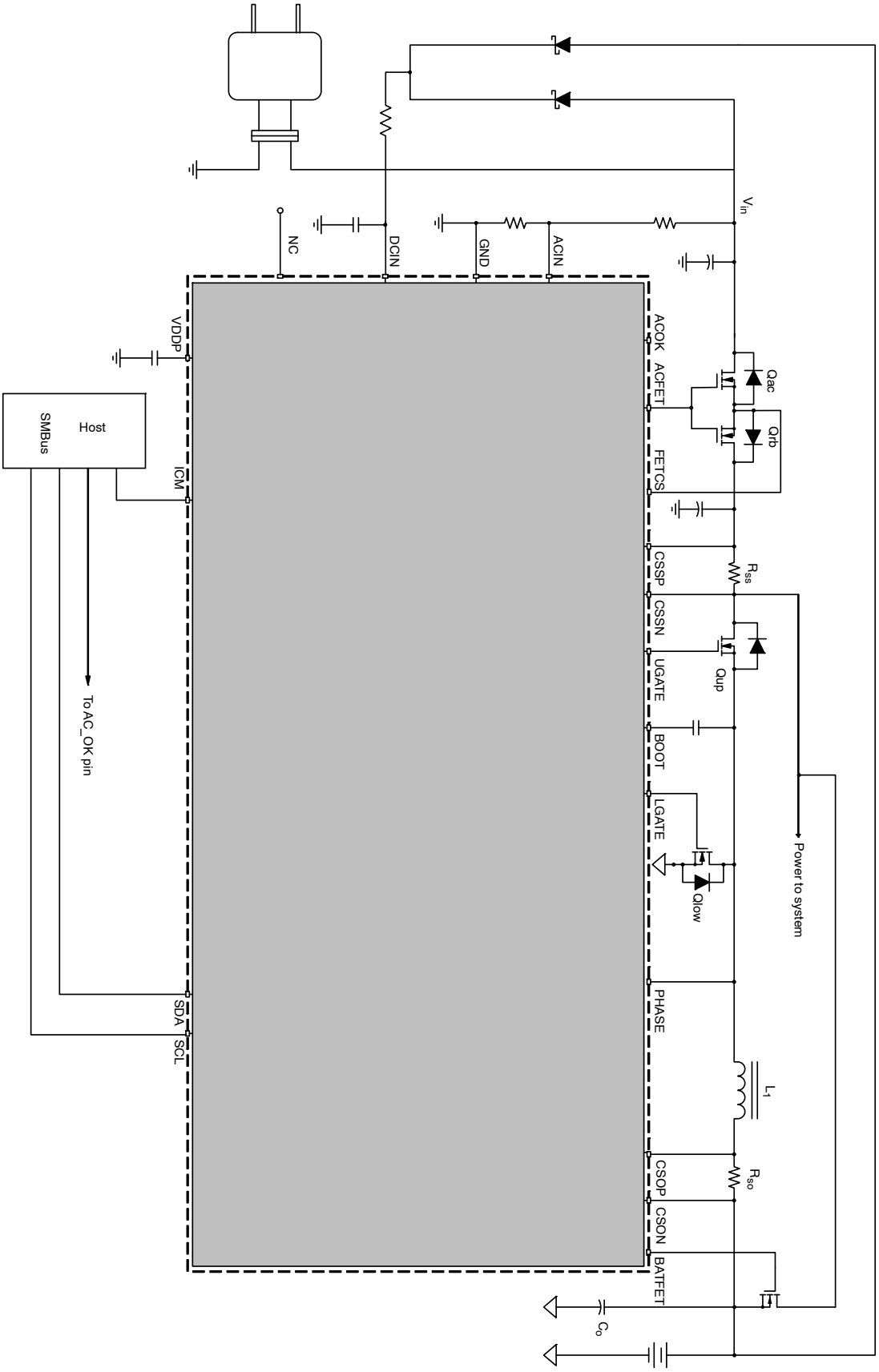



**Figure 1. System Diagram**

**Table 1. FUNCTIONAL PIN DESCRIPTION**

| Function | Pin | Description |
|---|---|---|
| ACOK | 5 | An open drain device indicates that status of the ac adaptor. Connecting a 10 kΩ resistor to external pull−up power supply. A high state indicates the adaptor is present. |
| ACFET | 4 | Gate drive to the series N−FET(s) from the ac adaptor to the system |
| ACIN | 6 | This Input detects the presence of the ac adaptor which is scaled by a voltage divider to determine if the adaptor is present and whether its output voltage is in the correct range for proper operation. |
| BOOT | 17 | The bootstrap pin connects to diode and capacitor to provide the drive to the upper gate. |
| CSON | 12 | The negative side of the output (charge) current sense resistor is connected to this node. This pin also plays the role of battery pack voltage sensing. |
| CSOP | 13 | The positive side of the output (charge) current sense resistor is connected to this node. |
| CSSN | 1 | The negative side of the input (adapter) current sense resistor is connected to this node. |
| CSSP | 2 | The positive side of the input (adapter) current sense resistor is connected to this node. |
| DCIN | 20 | This pin is the DC input to the chip. It provides bias power for the chip and also for the internal LDO. |
| GND | 14 | This is the ground reference pin for the chip. |
| ICM | 7 | The input current monitor provides a voltage signal that is the equivalent total input current or charge current drop across the sense resistor multiplied by a ratio programmed through ChargeOption() register. |
| FETCS | 3 | Common source pin of the series FET(s) from the AC adaptor to the system and charging circuit |
| LGATE | 15 | This pin provides the gate drive for the lower FET (synchronous rectifier) gate |
| PGND | PAD | This pin is the ground reference for the gate drive circuit. |
| PHASE | 19 | This pin connects to the switch node |
| SCL | 9 | This pin is an open−drain output for the SMBus Data I/O. An external pullup resistor should be connected according to SMBus specifications. |
| SDA | 8 | This pin is the SMBus Clock Input. An external pullup resistor should be connected according to SMBus specifications. |
| UGATE | 18 | This pin provides the gate drive for the upper FET (switch) gate. |
| BATFET | 11 | Gate drive to the external N−FET connecting the battery to the system rail |
| VDDP | 16 | This is the regulated supply for the switch drive. It should be bypassed with a >0.1 μF ceramic capacitor. |
| NC | 10 | Not connected. Recommended to be grounded. |

**Table 2. MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DCIN, CSSP, CSSN, CSOP, CSON, FETCS to GND<br>PHASE<br>ACFET, UGATE, BOOT, BATFET to GND<br>All other pins | $V_{max}$ | −0.3 to 30<br>−2.0 to 30<br>−0.3 to 36<br>−0.3 to 6.5 | V |
| Thermal Resistance, Junction−to−Air | $\theta_{JA}$ | 45 | °C/W |
| Operating junction temperature range | $T_j$ | 0 to 125 | °C |
| Ambient temperature range | $T_A$ | −10 to 100 | °C |
| Non−operating junction temperature range | $T_j$ | −55 to 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

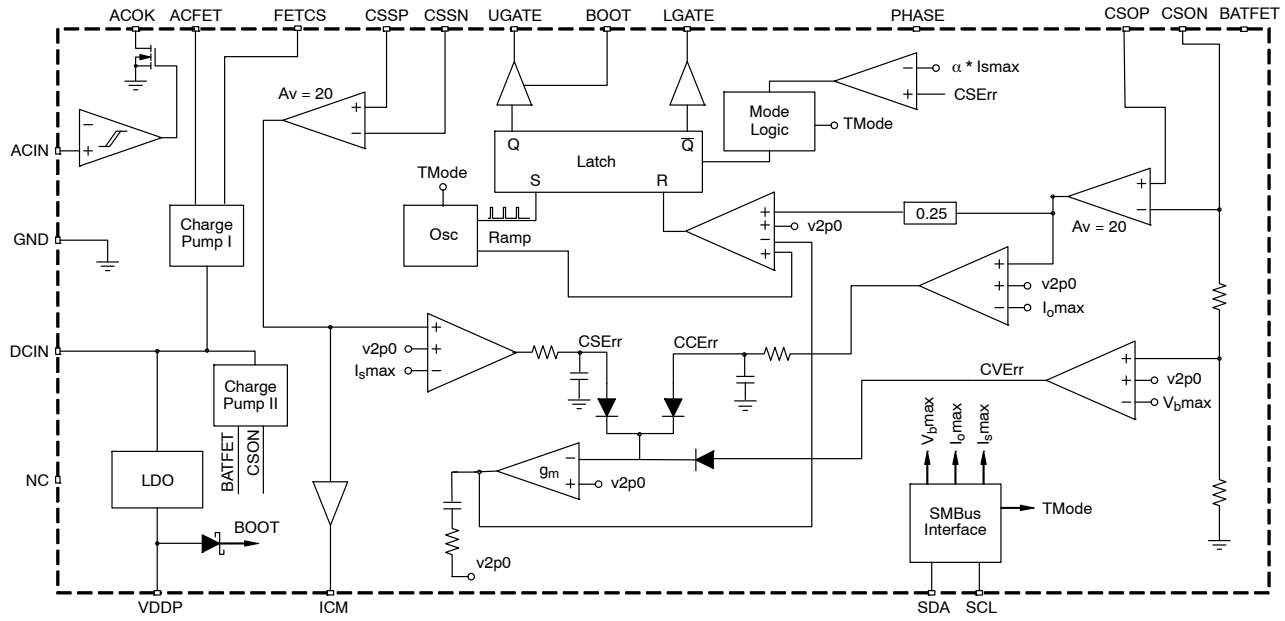



**Figure 2. Chip Block Diagram**

**Table 3. ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted: DCIN = 20.0 volts, $T_J$ = 0°C to +125°C, Rss = Rso = 10 mΩ)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OPERATING CONDITIONS** | | | | | |
| DCIN operating range | | 7 | | 25 | V |
| **CHARGING VOLTAGE** | | | | | |
| 4.2 V/Cell (ChargeVoltage() = 0x41A0H) 4 Cells | | 16.716 | 16.800 | 16.884 | V |
| | | −0.5 | | 0.5 | % |
| 4.2 V/Cell (ChargeVoltage() = 0x3130H) 3 Cells | | 12.529 | 12.592 | 12.655 | V |
| | | −0.5 | | 0.5 | % |
| 4.2 V/Cell (ChargeVoltage() = 0x20D0H) 2 Cells | | 8.350 | 8.400 | 8.450 | V |
| | | −0.6 | | 0.6 | % |
| **CHARGING CURRENT** | | | | | |
| ChargeCurrent()=0x1000H, 10 mΩ | | 39.53<br>−3.5 | 40.96 | 42.39<br>3.5 | mV<br>% |
| ChargeCurrent()=0x080H, 10 mΩ (Note 1) | | 0.64<br>−50.0 | 1.28 | 1.92<br>50.0 | mV<br>% |
| **ADAPTOR INPUT CURRENT** | | | | | |
| InputCurrent()=0x1000H, 10 mΩ | | 39.53<br>−3.5 | 40.96 | 42.39<br>3.5 | mV<br>% |
| InputCurrent()=0x0200H, 10 mΩ (Note 1) | | 3.84<br>−25.0 | 5.12 | 6.4<br>25.0 | mV<br>% |
| **CURRENT SENSE DIFF AMPS** | | | | | |
| Voltage Gain (input within ±100 mV) | $A_V$ | | 20 | | V/V |
| Input offset voltage (Note 1) | Ios | −1 | | 1 | mV |
| Common mode input range | Vicom | 7 | | 25 | V |

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**Table 3. ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted: DCIN = 20.0 volts, $T_J$ = 0°C to +125°C, Rss = Rso = 10 mΩ)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ICM OUTPUT** | | | | | |
| ICM output voltage range | | | | 5.5 | V |
| ICM output current | | 1 | | | mA |
| ChargeOption()bit9=0, current sense amplifier gain | | | 20 | | |
| ChargeOption()bit9=1, current sense amplifier gain | | | 40 | | |
| ChargeOption()bit5=0, adaptor current<br>ChargeOption()bit5=1, charge current | | | | | |
| ICM accuracy (Input referred) | | −1.2 | | 1.2 | mV |
| ICM accuracy (ChargeCurrent()=0x1000H, 10 mΩ) | | −3 | | 3 | % |
| **PWM & ERROR AMPLIFIERS** | | | | | |
| Oscillator Frequency | | | 750 | | kHz |
| **GATE DRIVE SUPPLY (VDDP)** | | | | | |
| Output Voltage ($I_{out}$ = 50 mA) | Vddp | 5.2 | 5.4 | 5.6 | V |
| Output Current (Note 1) | Ivddp | 40 | | | mA |
| Capacitor required for stability (Note 1) | Cvddp | 0.1 | | 4.7 | μF |
| **GATE DRIVERS** | | | | | |
| Lower Gate Drive Source Impedance, 10 mA | R_lgsrc | | 8 | 12 | Ω |
| Lower Gate Drive Sink Impedance, 10 mA | R_lgsnk | | 0.9 | 1.5 | Ω |
| Upper Gate Drive Source Impedance, 10 mA | R_ugsrc | | 6 | 12 | Ω |
| Upper Gate Drive Sink Impedance, 10 mA | R_ugsnk | | 0.65 | 1.3 | Ω |
| Driver Dead Time, 10 mA | Td | | 20 | | ns |
| **ACFET GATE DRIVER (Charge Pump)** | | | | | |
| Charge up rising time, 10 nF cap | | | 1.8 | 3 | ms |
| Gate driver voltage | Vacfet | 5.0 | | | V |
| Gate driver turn−off resistance | | | 9 | | kΩ |
| **BATFET GATE DRIVER (Charge Pump)** | | | | | |
| Charge up rising time, 10 nF cap | | | 1.8 | 3 | ms |
| Gate driver voltage | Vacfet | 5.0 | | | V |
| Gate driver turn−off resistance | | | 9 | | kΩ |
| **ACIN COMPARATOR AND ACOK** | | | | | |
| ACIN Adaptor Detect, Rising Threshold | | 1.96 | 2.00 | 2.04 | V |
| ACIN Adaptor Detect, Falling Hysteresis | | | 50 | | mV |
| ACIN wakeup threshold rising threshold | | | 0.63 | | V |
| ACIN wakeup threshold falling hysteresis | | | 0.05 | | V |
| ACOK Rising Delay (deglitch time, default) | | 100 | 175 | | ms |
| ACOK Voltage Drop (Low state, Isink = 1 mA) | | | 250 | 400 | mV |
| ACOK Leakage Current (Open drain, 3.3 V) | | | 0.5 | | μA |
| (ACOK deglitch time can be programmable by ChargeOption()bit15) | | 0: 175 ms(default);1: 1.4s | | | |

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**Table 3. ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted: DCIN = 20.0 volts, $T_J$ = 0°C to +125°C, Rss = Rso = 10 mΩ)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ACIN OVERVOLTAGE** | | | | | |
| ACIN Adaptor Detect, Rising Threshold | | 2.5 | 2.625 | 2.7 | V |
| ACIN Adaptor Detect, Falling Hysteresis | | | 50 | | mV |
| **DCIN COMPARATOR** | | | | | |
| DCIN Circuit Enable (Control circuits energized) Rising Threshold | | 6.0 | 6.4 | 6.9 | V |
| DCIN Circuit Enable, Falling Hysteresis | | 150 | 200 | 250 | mV |
| **PWM SOFT−START** | | | | | |
| Soft start current step | | | 128 | | mA |
| Soft start current step time | | | 240 | | μS |
| **BATTERY LOW COMPARATOR (BATLOWV)** | | | | | |
| Battery low falling threshold | | | 3.2 | | V |
| Battery low rising hysteresis | | | 200 | | mV |
| Battery low charge current limit (trickle charge limit) | | | 0.5 | | A |
| (Intermittent charge with 1 ms on time trickle charge and ~4 ms off time) | | | | | |
| **CHARGE OVERVOLTAGE PROTECTION** | | | | | |
| OVP Trip Level (Voltage in excess of set point) | | 102 | 104 | 106 | % |
| OVP Trip hysteresis | | | 2.0 | | % |
| **ADAPTOR OVERCURRENT** | | | | | |
| Adaptor overcurrent rising threshold, if ChargeOption:bit1 = 1 | | | 333 | | % |
| Adaptor overcurrent range (10mΩ sense resistor) | | 45 | | 150 | mV |
| Deglitch time | | | 4.2 | | ms |
| **CHARGE OVERCURRENT** | | | | | |
| overcurrent rising threshold, ChargeCurrent()=0x0xxxH | | | 60 | | mV |
| overcurrent rising threshold, ChargeCurrent()=0x01000H−0x17C0H | | | 90 | | mV |
| overcurrent rising threshold, ChargeCurrent()=0x01800H−0x1FC0H | | | 120 | | mV |
| **THERMAL SHUTDOWN** | | | | | |
| Thermal Trip Point, Temperature Increasing | $T_{SD}$ | | 170 | | °C |
| Thermal Shutdown Hysteresis, Temp Decreasing | $T_{Hyst}$ | | 30 | | °C |
| **DEVICE SUPPLY CURRENT** | | | | | |
| Operational Bias Current (Adaptor present, 2.625 V>ACIN>2.0 V, Charger enabled, non switching), Total current to DCIN, CSSP, CSSN | | | 1.5 | 3 | mA |
| Operational Bias Current (Adaptor disconnected, BATFET charge pump on, Total current into pins DCIN, CSSP, CSSN, CSON, CSOP, SWN) | | | | 300 | μA |
| Operational Bias Current (Adaptor disconnected, BATFET charge pump off, Total current into pins CSSP, CSSN, CSON, CSOP, SWN) | | | | 100 | μA |
| **HIGH SIDE FAULT (HS_FAULT)** | | | | | |
| High side OCP threshold, CSSN−PHASE ChargeOption()bit8=1 | | | 610 | | mV |
| ChargeOption()bit8=0, function disabled | | | | | |
| **LOW SIDE FAULT (LS_FAULT)** | | | | | |
| Low side OCP threshold, PHASE−GND ChargeOption()bit7=0 | | | 135 | | mV |
| ChargeOption()bit7=1 | | | 230 | | |

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**Table 3. ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted: DCIN = 20.0 volts, $T_J$ = 0°C to +125°C, Rss = Rso = 10 mΩ)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DCIN to CSON** | | | | | |
| DCIN to CSON falling threshold | | | 110 | | mV |
| DCIN rising hysteresis | | | 160 | | mV |
| **CSSN to CSON** | | | | | |
| CSSN falling, CSSN to BAT falling threshold | | | 220 | | mV |
| CSSN rising hysteresis | | | 90 | | mV |
| **BATTERY DEPLETION COMPARATOR** | | | | | |
| ChargeOption()bit[12:11]=00 | | | 59.19 | | % |
| ChargeOption()bit[12:11]=01 | | | 62.65 | | % |
| ChargeOption()bit[12:11]=10 | | | 66.55 | | % |
| ChargeOption()bit[12:11]=11 | | | 70.97 | | % |
| Battery depletion rising hysteresis | | | 340 | | mV |
| **SMBUS TIMING ($V_{DD}$ = 2.7 to 5.5 V)** (Note 1) | | | | | |
| SCLK/SDATA Rise Time | $t_r$ | | | 1 | μs |
| SCLK/SDATA Fall Time | $t_f$ | | | 300 | ns |
| SCLK Pulse Width High | $t_{W(Hi)}$ | 4.0 | | 50 | μs |
| SCLK Pulse Width Low | $t_{W(Lo)}$ | 4.7 | | | μs |
| Setup Time for START Condition | $t_{SU(STA)}$ | 4.7 | | | μs |
| START Condition Hold Time After Which First Clock Pulse is Generated | $t_{H(STA)}$ | 4.0 | | | μs |
| Data Setup Time | $t_{SU(DAT)}$ | 250 | | | ns |
| Data Hold Time | $t_{H(DAT)}$ | 300 | | | ns |
| Setup Time for STOP Condition | $t_{SU(STOP)}$ | 4.0 | | | μs |
| Bus Free Time Between START and STOP Condition | $t_{BUF}$ | 4.7 | | | μs |
| Clock Frequency | $f_{S(CL)}$ | 10 | | 300 | kHz |
| **HOST COMMUNICATION FAILURE** | | | | | |
| Watchdog Timeout Period | $t_{(WD)}$ | 140 | 170 | 210 | s |
| (See ChargeOption()bit[14:13]) | | | | | |
| **LOGIC INPUT (SDATA,SCLK)** | | | | | |
| Input low | VIL | | | 0.8 | V |
| Input High | VIH | 2.1 | | | V |
| **LOGIC OUTPUT (SDATA)** | | | | | |
| Output saturation voltage, 3 mA current | | | | 0.4 | V |

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## Circuit Descriptions

### Soft−start

This chip has two soft−start circuits built in to its circuitry to limit the inrush current and the reduce overshoot of the system.

When the adaptor is first plugged into the system, charge has not started. The voltage of ACFET pin rises over a period of several ms to slow the turn on of the system FET(s). The ACFET−FETCS voltage remains around turn−on threshold allowing the FET(s) Qac and Qrb working in their saturation region. The Cgs and Cgd capacitance of the external adaptor FETs need to be carefully selected to control this soft turn−on slew rate. The output voltage of the n−channel FET will then follow in a linear manner at a gate threshold voltage below the voltage on the ACFET gate pin.

After the external FETs are fully turned on and every time charge is enabled, the charger automatically steps the charge current up softly in 128 mA increments in a fixed time step until it reaches to the charge limit current. This charge current soft start makes sure the battery energized in its safe manner.

### Current Regulators

There are two current monitors required for this chip. The resistor Rso measures the charge current into the battery. The full−scale limit for this shunt resistor is 80 mV and can be reduced in 0.64 mV steps. A highly accurate amplifier detects the voltage across the shunt resistor. The actual current level is dependent on the value of the Rso, eg. 10 mΩ.

The Rss resistor monitors the adaptor input current. It has a full scale reading of 80 mV and can be reduced in 1.28 mV steps. Either the adaptor current or charge current information is available at the ICM pin with 20x or 40x ratio, this is programmable from the ChargeOption() register.

If the total adaptor input current reaches its programmed level, the reference for the charging current will be reduced by an appropriate amount to maintain a constant level for the system current. If the battery voltage drops below BATLOWV voltage, the charger will enter a trickle charge cycle: it will reduce the current level to 128 mA and then soft start to 0.5 A (Rso = 10 mΩ) when the BATLOWV condition persists. This can last for 1 ms and the charge will stop for 4~5 ms, and then charge will restart with another BATLOWV trickle cycle. Once the battery voltage is over BATLOWV voltage, the softstart will continues and go into the normal charge cycle.

### Gate Drive Regulator and LDO

The VDDP LDO can source a minimum 40 mA to the charge pump gate drive circuitry and for the high and low−side gates. It also power the rest of logic circuit while the adapter is present. A bypass capacitor larger than 0.1 μs should be applied to the VDDP output for the stability.

### Adaptor Detection

The ACIN pin monitors the DC output of the ac adaptor or the battery pack and allows the system to turn on when sufficient voltage is present. The DCIN pin is also monitored and when the voltage is at 6.4 volts or greater, the internal circuits will become energized.

When the voltage at the ACIN pin is over 0.6 V wakeup level, the internal LDO will start working with a valid VDDP output. SMbus circuit will be ready to communicate with host controller. But ACOK pin remains low indicating adaptor is not ready.

When the voltage at the ACIN pin reaches 2.00 volts, DCIN−CSON>275 mV and the deglitch time (175 ms or 1.4 s) is over, all functions are enabled, including all the comparators, amplifiers, charge pump and gate drivers to the external switches. The ACOK pin changes to a high state to indicate that the adaptor is present and has sufficient voltage to allow proper operation. The charge pump circuit ramps the gate to source voltage (ACFET−FETCS) up on external adaptor FETs until their gate voltage reaches the full scale voltage and the FETs are fully on. The external FETs can be one or two back−to−back N channel FETs.

When the ACIN voltage is over 2.625 V, it is considered as overvoltage condition for the adapter input, ACOK will changes to a low state and ACFET will be pulled down.

### PWM Control Circuit

The control circuit for the NCP3800V is a fixed frequency, current mode control PWM.

At light loads, the propagation delays of the controller and gate drive will tend to overcharge the battery. In the event that the battery charge voltage exceeds the set point by several milivolts, the comp signal will go low. When this occurs the oscillator will not trigger the gate drive and the drive will remain off until the comp pin moves up to regulation range. This reduces the switching frequency and improves efficiency. In order to let the boost cap to have enough charge for the next high side turn on event, a detection circuit has been implemented once the BST to phase node voltage is less than 4.0 V. Once it is detected, low side FET will be turned on to charge the boost cap voltage up.

### Battery Overvoltage Protection

The overvoltage protection circuit monitors the output voltage and if it exceeds the set point by 4% for more than 1 μs, the drive will be removed from both the upper and lower FETs. An internal current source will be turned on to discharge the output. If OVP lasts for over 30 ms, charge controller will be latched off, it will remain off until the power is recycled.

### Adaptor Overvoltage Protection

If ACIN voltage is higher than 2.625 V, it is considered as adaptor over voltage. ACOK will be pulled low and charge will be disabled. ACFET will be turned off to disconnect the adaptor from the system and charge circuit. BATFET will be turned on instead if a valid battery input is presented.

### System Power Selection

The NCP3800V automatically switches adapter or battery power to system. The battery is connected to system if the battery exists and its voltage crosses UVLO thershold. The battery is disconnected from system and the adapter is connected to system after default time delay if ACOK goes HIGH.

ACFET and FETCS provide a true differential drive to the external N−channel MOSFET(s) between the adaptor and the system. The back to back N−channel FETs provides an inrush current control, also prevents input current from flowing in reverse direction.

BATFET and CSON provide another differential drive to the external N−channel MOSFET connected between the battery and the system. When it is off, the BATFET will be pulled down to the same level of battery voltage.

### Battery LEARN Cycle

A battery LEARN cycle can be activated through SMBus command (ChargeOption() bit[6]=1 enable LEARN cycle, bit[6]=0 disable LEARN cycle). When LEARN is enabled with adapter FETs connected, the system power selector logic is over−driven to switch to battery by turning off adapter FETs and turning on battery FET if the system voltage falls below the battery voltage. LEARN function allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge/charge cycle. The controller automatically exits LEARN cycle when the battery voltage is below battery depletion threshold. The system switches back to adapter input by turning off the battery FET immediately and turning on the adapter FETs. After LEARN cycle, the LEARN bit is automatically reset to 0. The battery depletion threshold can be set to 59.19%, 62.65%, 66.55%, and 70.97% in proportion to the voltage regulation level via SMBus command (ChargeOption() bit[12:11]).

### Adaptor Input Over Current Protection

Set by ChargeOption() bit1, the default is 3.33x of input current DAC set point. After ~4 ms blank time, the adapter FET(s) will turned off and ACOK going low. The system will be latched and power on reset is needed to allow the adapter FETs to turn on again.

### Charge Over Current Protection

It is a cycle by cycle non−latched peak current protection. OCP threshold is automatically set to 6 A, 9 A, 12 A based on the charge current register value. Proper inductor should be selected to prevent OCP triggered in normal operation due to higher inductor ripple current.

### Battery Over Voltage Protection

Both high side and low side FETs will be turned off if the battery voltage exceeds 104% of the regulation voltage set−point. A 4 mA current sink from the switch node to ground is on to discharge the output. If battery overvoltage lasts more than 30 ms, charger will be completely disabled.

### Battery Shorted to Ground (BATLOWV)

The NCP3800V will limit inductor current if the battery voltage falls below BATLOWV. When this happens, the charger will reduce the charge current level to 128 mA and charge will soft start to 0.5 A when the BATLOWV conditions persist. After ~1 ms or trickle charge, the charge will stop for 4~5 ms, and then restart another cycle of trickle charge. If the battery voltage exceeds BATLOWV, the system will exit trickle charge and resume normal charge through internal control loop.

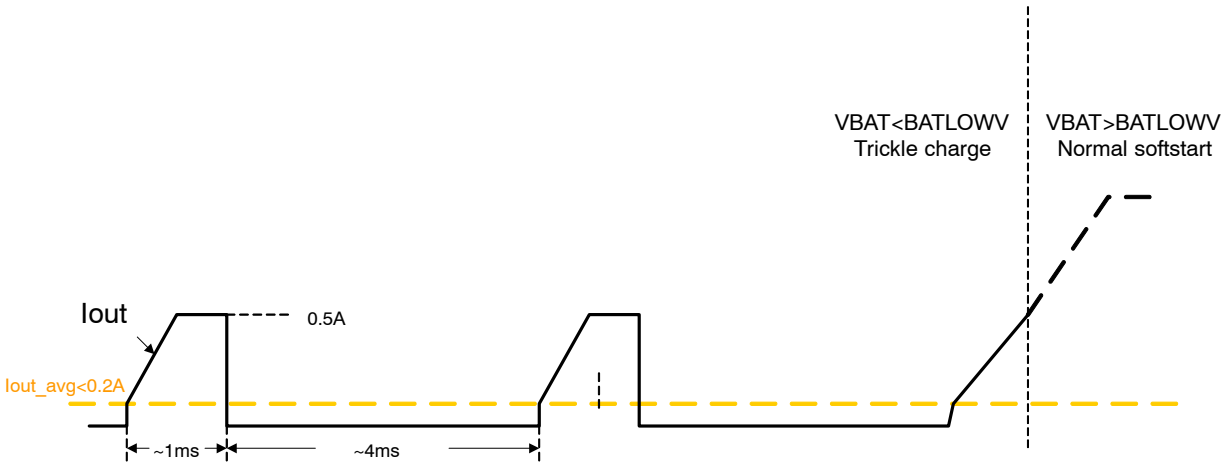



**Figure 3. Charge Current under BATLOWV Condition**

This feature prevents any overshoot current in inductor which can saturate inductor or damage MOSFETs when the battery is deeply discharged or shorted.

### High Side(HS_FAULT)/Low Side MOSFET short (LS_FAULT), Inductor Short

Besides cycle by cycle charger Overcurrent protection, NCP3800V also provides short circuit protection via sensing the voltage drop on the Rds(on) of the high side and low side FETs after a certain amount of blanking time. The low side MOSFET fault (LS_FAULT) threshold can be adjusted through the ChargeOption()bit[7] (0:135mV or 1:230 mV). The high side MOSFET fault(HS_FAULT) threshold can be set to 610 mV or disabled through ChargeOption()bit[8]. They are cycle by cycle protection, once triggered, the driver signal will be turned off within the cycle; if the high side fault or low side fault lasts for 7 consecutive cycles, the charger will be latched off. A power on reset (DCIN) or ACIN below 0.6 V toggling is required to reset the charger.

### Thermal Shutdown

The charger converter turns off for self−protection whenever the junction temperature exceeds the 170°C. The charger stays off until the junction temperature falls below 140°C. During thermal shut down, the converter gate drivers will be turned off. Once the temperature falls below 135°C, charge can be resumed with soft start.

### Enable and Disable Charging

The following conditions must be valid before charging is enabled:

- Charging enabled through the SMBus, all the three regulation register values are valid;
- ACOK valid, ACIN >2.0V after deglitch time, ACFETs fully turned on;
- CSON is less than the battery OVP threshold
- VDDP is valid;
- Thermal Shutdown (TSHUT) is not active;
- Input current is less than the input current OCP limit;

Any of the following conditions stop the charge cycle:

- Charging is disabled through SMBus, one of the three regulation limit DAC set to 0 or out of range;
- ACOK is pulled low (Overvoltage or Undervoltage);
- ACFETs off;
- CSON voltage is over the battery OVP threshold;
- Input current is over the input current OCP limit;
- Inductor, high side/low side MOSFET OCP;
- TSHUT IC temperature threshold is reached;
- Watch dog timer expired;

## Theory of Operation

### Battery Voltage Regulator

The voltage regulation loop is the controlling loop when the battery charging current demand is less than the programmed current limit level for the charger. The voltage regulation point is set by entering data into the 0x15 register. On startup, this register defaults to 0000 which inhibits operation of the charger. It must be set by an SMBus code before the charger can commence operation.

The battery voltage is set using a high−accuracy reference and an 11 bit DAC. It can be set at a level from 1.024 to 19.2 volts, in 16 mV increments. The actual setting used depends on the number of cells, the chemistry of the battery and the desired life/charge tradeoff for the battery.

It is recommended to place a 0.1 μF ceramic capacitor with leads as short as possible between the CSON and GND pins to minimize the noise on this pin and thus improve regulation.

### Battery Current Regulator

The maximum battery charging current is set by entering SMBus data into the 0x14 register. This register requires a 16 bit entry with 7 bits to program the 7 bit DAC. The other bits should all be zero. This register defaults to 0000 and must be programmed to a current level between 128 mA and 8.064 A to begin charger operation.

The currents are based on a 10 mΩ sense resistor. Other values will change the current by an amount based on the ratio of 10 mΩ/Rsense; e.g. a 12 mΩ resistor with a 4 amp current limit code would then become 4.0 A x (.010 Ω / .012 Ω) = 3.33 A.

### Input Current Regulator

The system input current is set by entering SMBus data into the 0x3F register. This register requires a 16 bit entry with 6 bits to program the 6 bit DAC. The other bits should all be zero. This register defaults to 1000H. Based on a 10 mΩ sense resistor, this current can be programmed from 128 mA to 8.064 A.

Total input current is the sum of system supply current and charge current. If the If the input current exceed the set input current limit, the charge current will be reduced to guarantee the system supply input.

### SMBus™ Interface

The NCP3800V operates as a slave, receiving control inputs from the host through the SMBus interface. The NCP3800V uses a simplified subset of the commands documented in System Management Bus Specification V1.1. The NCP3800V uses the SMBus Read−Word and Write−Word protocols to communicate with the smart battery. The NCP3800V performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the NCP3800V has two identification registers a 16−bit device ID register (0xFFH) and a 16−bit manufacturer ID register (0xFEH).

SMBus communication is enabled under the following conditions:

- DCIN voltage is above UVLO threshold;
- ACIN voltage is above 0.6 V;

The data (SDA) and clock (SCL) pins have Schmitt−trigger inputs that can accommodate slow edges. Choose pull−up resistors (10 kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a START condition, which is a high−to−low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low−to−high transition on SDA, while SCL is high. The bus is then free for another transmission. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8−bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the NCP3800V because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The NCP3800V supports the charger commands as described in the tables of the next section.

a) Write-Word Format

| S | SLAVE ADDRESS | W | ACK | COMMAND BYTE | ACK | LOW DATA BYTE | ACK | HIGH DATA BYTE | ACK | P |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 BITS | 1b | 1b | 8 BITS | 1b | 8 BITS | 1b | 8 BITS | 1b | |
| | MSB LSB | 0 | 0 | MSB LSB | 0 | MSB LSB | 0 | MSB LSB | 0 | |

Preset to 0b0001001 ChargeCurrent() = 0x14H D7 D0 D15 D8
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
ChargeOption() = 0x12H

b) Read-Word Format

| S | SLAVE ADDRESS | W | ACK | COMMAND BYTE | ACK | S | SLAVE ADDRESS | R | ACK | LOW DATA BYTE | ACK | HIGH DATA BYTE | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 7 BITS | 1b | 1b | 8 BITS | 1b | | 7 BITS | 1b | 1b | 8 BITS | 1b | 8 BITS | 1b | |
| | MSB LSB | 0 | 0 | MSB LSB | 0 | | MSB LSB | 1 | 0 | MSB LSB | 0 | MSB LSB | 1 | |

Preset to 0b0001001 ChargeCurrent() = 0x14H Preset to 0b0001001 D7 D0 D15 D8
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
ChargeOption() = 0x12H

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

**Figure 4. SMBus Read and Write Protocols**

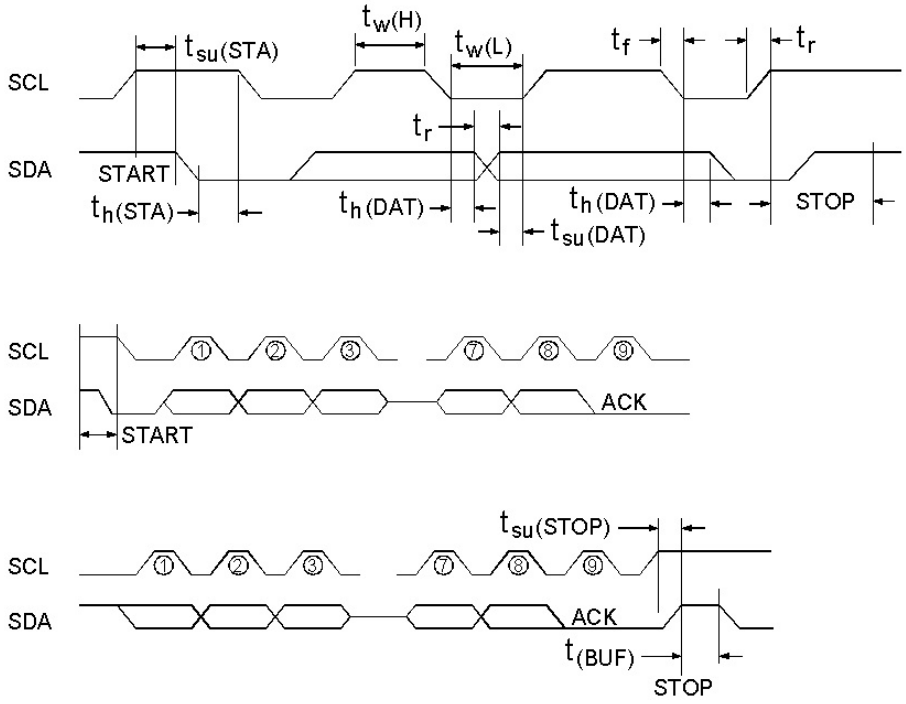



**Figure 5. SMBus Timing Diagrams**

**Table 4. CHARGE COMMAND REGISTER**

| Register Address | Register Name | R/W | Description | Default |
|---|---|---|---|---|
| 0x12 | Charge Option () | R/W | Set charging options | 0x7902 |
| 0x14 | Charge Current () | R/W | 7−bit battery charging current limit | 0x0000 (0 A) |
| 0x15 | Charge Voltage () | R/W | 11−bit battery charging voltage limit | 0x0000 (0 V) |
| 0x3F | Input Current () | R/W | 6−bit input current limit | 0x1000 (4.096 A) |
| 0xFE | Manufacturer ID () | R | Manufacturer identification | 0x0007 |
| 0xFF | Device ID () | R | Device identification | 0x0007 |

## Voltage Regulation

The output voltage compliance is set in the 0x15 register via the SMBus. The minimum voltage level is 1.024 volts and the maximum is 19.2 volts with 16 mV of resolution. To set the voltage level, a 16 bit command must be issued using the data format in the following table.

**Table 5. CHARGE VOLTAGE REGISTER (Register 0x15)**

| Bit | Bit Name | Description |
|---|---|---|
| 0 | | Not Used |
| 1 | | Not Used |
| 2 | | Not Used |
| 3 | | Not Used |
| 4 | Charge Voltage, DACV 0 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 16 mV to charger voltage |
| 5 | Charge Voltage, DACV 1 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 32 mV to charger voltage |
| 6 | Charge Voltage, DACV 2 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 64 mV to charger voltage |
| 7 | Charge Voltage, DACV 3 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 128 mV to charger voltage |
| 8 | Charge Voltage, DACV 4 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 256 mV to charger voltage |
| 9 | Charge Voltage, DACV 5 | 0 = Adds 0 mV to charger voltage, 1024 mV min<br>1 = Adds 512 mV to charger voltage |
| 10 | Charge Voltage, DACV 6 | 0 = Adds 0 mV to charger voltage<br>1 = Adds 1,024 mV to charger voltage |
| 11 | Charge Voltage, DACV 7 | 0 = Adds 0 mV to charger voltage<br>1 = Adds 2,048 mV to charger voltage |
| 12 | Charge Voltage, DACV 8 | 0 = Adds 0 mV to charger voltage<br>1 = Adds 4,096 mV to charger voltage |
| 13 | Charge Voltage, DACV 9 | 0 = Adds 0 mV to charger voltage<br>1 = Adds 8,192 mV to charger voltage |
| 14 | Charge Voltage, DACV 10 | 0 = Adds 0 mV to charger voltage<br>1 = Adds 16,384 mV to charger voltage |
| 15 | | Not used. |

### Charging Current Limit

The battery charging current limit is set in the 0x14 register via the SMBus. The minimum current level is 128 mA with a maximum of 8.064 A with a 64 mA resolution. These values are based on a 10 mΩ sense resistor in the charge current path. Set the charge current to 0 to terminate charging.

The NCP3800V monitors the battery voltage and will reduce the charging current to 128 mA if the battery voltage is less than 2.5 volts per cell.

**Table 6. CHARGE CURRENT LIMIT REGISTER (Register 0x14, 10 mΩ sense resistor)**

| Bit | Bit Name | Description |
|---|---|---|
| 0 | | Not Used |
| 1 | | Not Used |
| 2 | | Not Used |
| 3 | | Not Used |
| 4 | | Not Used |
| 5 | | Not Used |
| 6 | Charge Current, DACI 0 | 0 = Adds 0 mA to charger current<br>1 = Adds 64 mA to charger current |
| 7 | Charge Current, DACI 1 | 0 = Adds 0 mA to charger current<br>1 = Adds 128 mA to charger current |
| 8 | Charge Current, DACI 2 | 0 = Adds 0 mA to charger current<br>1 = Adds 256 mA to charger current |
| 9 | Charge Current, DACI 3 | 0 = Adds 0 mA to charger current<br>1 = Adds 512 mA to charger current |
| 10 | Charge Current, DACI 4 | 0 = Adds 0 mA to charger current<br>1 = Adds 1,024 mA to charger current |
| 11 | Charge Current, DACI 5 | 0 = Adds 0 mA to charger current<br>1 = Adds 2,048 mA to charger current |
| 12 | Charge Current, DACI 6 | 0 = Adds 0 mA to charger current<br>1 = Adds 4,096 mA to charger current, 8,064 mA max |
| 13 | | Not Used. |
| 14 | | Not Used. |
| 15 | | Not Used. |

### Adaptor Input Current Limit

The wall adaptor current limit is set in the 0x3F register via the SMBus. The adaptor current is made up of the system current plus the charging current. Since the system current can vary over a wide range, this current limit circuit functions to reduce the charging current in order to keep the adaptor current at a level that is below the maximum current setting for the charger.

The minimum current level is 128 mA with a maximum of 8.064 A with a 128 mA resolution. These values are based on a 10 mΩ sense resistor in the charge current path.

**Table 7. INPUT CURRENT LIMIT REGISTER (Register 0x3F, 10 mΩ sense resistor)**

| Bit | Bit Name | Description |
|---|---|---|
| 0 | | Not Used |
| 1 | | Not Used |
| 2 | | Not Used |
| 3 | | Not Used |
| 4 | | Not Used |
| 5 | | Not Used |
| 6 | | Not Used |
| 7 | Input Current, DACS 0 | 0 = Adds 0 mA to input current<br>1 = Adds 128 mA to input current |

**Table 7. INPUT CURRENT LIMIT REGISTER (Register 0x3F, 10 mΩ sense resistor)**

| Bit | Bit Name | Description |
|---|---|---|
| 8 | Input Current, DACS 1 | 0 = Adds 0 mA to input current<br>1 = Adds 256 mA to input current |
| 9 | Input Current, DACS 2 | 0 = Adds 0 mA to input current<br>1 = Adds 512 mA to input current |
| 10 | Input Current, DACS 3 | 0 = Adds 0 mA to input current<br>1 = Adds 1,024 mA to input current |
| 11 | Input Current, DACS 4 | 0 = Adds 0 mA to input current<br>1 = Adds 2,048 mA to input current |
| 12 | Input Current, DACS 5 | 0 = Adds 0 mA to input current<br>1 = Adds 4,096 mA to input current |
| 13 | | Not Used. |
| 14 | | Not Used. |
| 15 | | Not Used. |

**Charge Options**

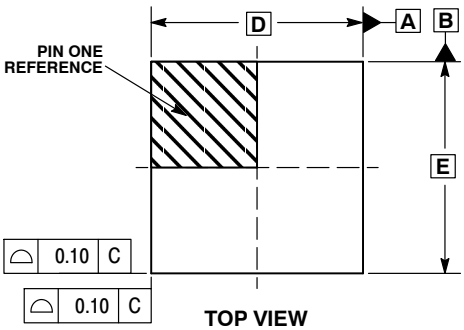
By writing ChargeOption() (0x12H), users are allowed to change the several changer options after power on reset. Bit 4 and Bit 2 are read only bits for the users to visit the charger status.

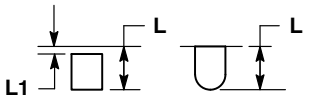
**Table 8. CHAREGE OPTION REGISTOR (Register 0x12)**

| Bit | Bit Name | Description |
|---|---|---|
| 15 | ACOK deglitch time | 0: 175 ms (default at POR);1: 1.4S |
| 14:13 | Watchdog Timer | 00: Disable the timer<br>01: Enabled, 44S<br>10: Enabled, 88s<br>11: Enabled, 175s (default) |
| 12:11 | BAT Depletion Comparator | 00: 59.19%<br>01:62.65%<br>10: 66.55%<br>11:70.97% |
| 10 | | Not Used |
| 9 | ICM Current amplifier gain factor | 0: 20x (default)<br>1: 40x |
| 8 | IFAULT_HI | 0: disabled;<br>1: 610 mV(default) |
| 7 | IFAULT_LO | 0: 135 mV<br>1: 230 mV |
| 6 | LEARN Enable | 0: disable learn (default)<br>1: enable learn |
| 5 | ICM selection | 0: ICM is 20x or 40x adaptor input current amp output (default)<br>1: ICM is 20x or 40x charger current amp output |
| 4 | AC adapter indication (Read only) | 0: ACIN beyond (2.0 V, 2.625 V) (default)<br>1:ACIN within (2.0 V, 2.625 V) |
| 3 | N/A | Always set to 0 |
| 2 | N/A | Always set to 0 |
| 1 | Adaptor OC threshold | 0: function is disabled<br>1: 3.33x input current regulation limit (default) |
| 0 | Charge Inhibit | 0: Enable charging (default)<br>1: Disable charging |

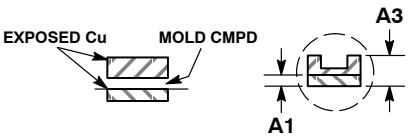
## PACKAGE DIMENSIONS

**QFN20 3.5x3.5, 0.5P**
CASE 485CP
ISSUE O

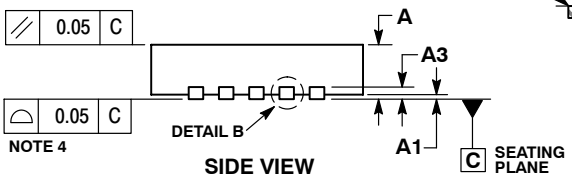



**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**



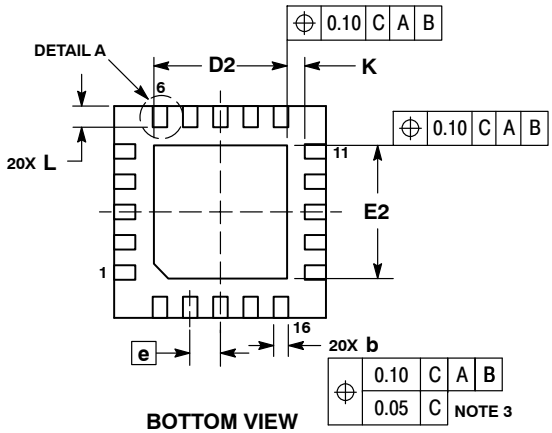

**DETAIL B**
**ALTERNATE CONSTRUCTIONS**




**SIDE VIEW**

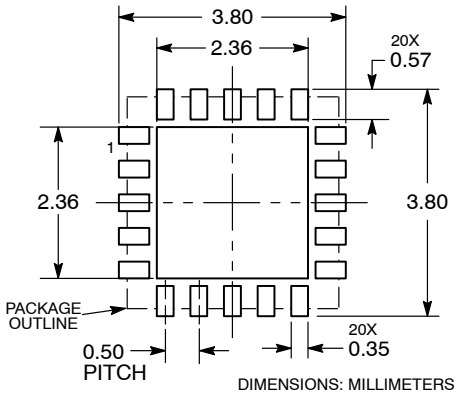
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 3.50 BSC | |
| D2 | 2.10 | 2.30 |
| E | 3.50 BSC | |
| E2 | 2.10 | 2.30 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.45 |
| L1 | 0.00 | 0.15 |




**BOTTOM VIEW**

**RECOMMENDED MOUNTING FOOTPRINT**

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